Form PTO-1390 (REV 10-97) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 19730-000110US

U.S. APPLICATION NO (If known, see 37 C.F.R. 1.5): 09/937680

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US00/08562	28 March 2000	29 March 1999

TITLE OF INVENTION

METHOD AND APPARATUS FOR PROVIDING PULSE WIDTH MODULATION

APPLICANT(S) FOR DO/EO/US

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Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☐ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☒ is not required, as the application was filed in the United States receiving Office (RO/US)

6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☒ Amendments as to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary examination Report under PCT Article 36 (35 U.S.C. 371(c)(5))

Items 11. to 16. below, concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information: Small Entity Statement, Power of Attorney, Certificate of Express Mailing

U.S. APPLICATION NO (If known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
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17. ☒ The following fees are submitted:		CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5)):			
Search Report has been prepared by the EPO or JPO	840.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482)	670.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2)	760.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO	970.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =		**$ 670.00**	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).		**$ 130.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	30-20=	10	x $18.00	**$ 180.00**	
Independent Claims	6-3=	3	x $7800	**$ 234.00**	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $260.00	**$**	
TOTAL OF ABOVE CALCULATIONS =				**$ 1214.00**	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 C.F.R. 1.9, 1.27, 1.28).				**$ 607.00**	
SUBTOTAL =				**$ 607.00**	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)). +				**$**	
TOTAL NATIONAL FEE =				**$**	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				**$ 40.00**	
TOTAL FEES ENCLOSED =				**$647.00**	
				Amount to be refunded:	**$**
				charged	**$**

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 20-1430 in the amount of **$ 647.00** to cover the above fees.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-1430. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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REGISTRATION NUMBER

Method and Apparatus for Providing Pulse Width Modulation

CROSS-REFERENCES TO RELATED APPLICATIONS

This patent claims the benefit of U.S. Provisional Applications 60/126,770 filed on March 29, 1999, 60/164,083 filed November 5, 1999, 60/163,707 filed November 5, 1999, 60/164,326 filed November 7, 1999.

BACKGROUND OF THE INVENTION

This invention relates generally to power supply circuits. More particularly, this invention relates to unipolar pulse width modulated power supply circuits.

Pulse width modulation is a technique that is utilized to power a variety of loads, including induction motor loads, lighting loads, etc. For example, with respect to induction motor loads, variable speed drives now exist that allow for the control of these induction motors. The variable speed drives (VSD's) allow the induction motors to be operated at a variety of different speeds. Furthermore, the speed of the induction motors can be monitored and the VSD output can be corrected via feedback from the sensed motor characteristic. Thus, an induction motor which previously operated at only a few set speeds, can now be operated throughout a spectrum of different speeds, particularly very low speeds.

Pulse Width Modulation (PWM) is a general technique in which a DC signal is pulsed out to a load. The magnitude of each DC pulse remains generally constant from pulse to pulse; however, the width of pulses will typically vary. In one PWM technique, for example, the pulse widths and pulse spacings are arranged so that their weighted average approaches a sine wave. This sine wave is considered to have a "fundamental" frequency, whereas the frequency of the pulses is referred to as the "carrier frequency." A variety of methods for generating a pulse width modulated signal can be seen in "A Centroid-Based PWM Switching Technique for Full-Bridge Inverter Applications" by Ali Yazdian-Varjani et al., in IEEE Transactions on Power Electronics, Vol. 13, No. 1, January 1998.

At least two different types of pulse width modulation are in use. The more common is bipolar pulse width modulation. In bipolar pulse width modulation a waveform such as that shown in Fig. 6 is generated. As can be seen in Fig. 6, the PWM

waveform extends between –Vdc and +Vdc during each transition. A second type of PWM is known as unipolar pulse width modulation. In unipolar pulse width modulation, a waveform such as that shown in Fig. 5 is produced. As can be seen in Fig. 5, the unipolar PWM waveform transitions between the reference voltage, e.g., zero volts, and +Vdc or –Vdc, depending upon the polarity of the output signal.

To generate the bipolar pulse width modulation signal a circuit such as that shown in Figures 7 and 8 is utilized. As can be seen in Fig. 7, an H-bridge inverter circuit is configured such that switches SW11 and SW22 are placed in a conducting position while switches SW12 and SW21 are placed in non-conducting position. This establishes a positive voltage across the load. Then, switches SW11 and SW22 are opened and switches SW12 and SW21 are closed, as shown in Fig. 8. Thus, four switch transitions are required to accomplish a transition of the PWM waveform.

Bipolar pulse width modulation waveforms have several drawbacks. The large magnitude of the transition, e.g., 2Vdc, results in a large voltage overshoot. As a result, the load can be damaged by this large voltage overshoot. Furthermore, one must switch all of the switches to accomplish a single transition of the PWM waveform. In addition, current spikes and associated electromagnetic interference (emi) can result. Thus, bipolar pulse width modulated signals are less preferable than unipolar pulse width modulated waveforms.

In the Yazdian-Varjani, et al. article, the authors outlined an algorithm for generating a unipolar pulse width modulated waveform. Namely, it required using a first set of switches in the H-bridge inverter to control the polarity of the output waveform while utilizing a second set of switches to control the modulation of the DC signal, e.g., the width and spacing of pulses. Thus, the switches responsible for controlling the width and spacings of each pulse incurred much more switching than the two switches responsible for controlling the polarity of the signal applied to the load. This method still has several disadvantages due to the mismatch of the characteristics of switches.

Hence there is still a need for a pulse width modulation scheme that overcomes some of the disadvantages inherent to bipolar PWM as well as some of the drawbacks inherent to existing unipolar PWM schemes. Furthermore, there is simply a need for an additional scheme for generating a unipolar PWM output signal.

SUMMARY OF THE INVENTION

The present invention overcomes disadvantages of earlier PWM designs and provides inventive subject matter which satisfies needs left unfulfilled by the current state of the art.

One embodiment of the invention is advantageous in that it provides a pulse width modulation scheme that reduces the number of switching transitions required to accomplish a transition of the pulse width modulation output waveform.

Another advantage, is that one embodiment of the invention allows unipolar pulse width modulation to be accomplished while spreading the wear and tear of the switching transitions to all four switches in an inverter bridge.

Yet another embodiment of the invention is advantageous in that it provides a pulse width modulation scheme in which a switching circuit is operable to not only reverse the polarity of the pulse width modulation output waveform but also to produce the pulse width modulation waveform.

Similarly, an embodiment of the invention provides the advantage of using two switching circuits, wherein each is separately operable to produce a pulse width modulated waveform.

In accordance with one embodiment of the invention, a power supply system is provided comprising an input to receive a DC voltage signal, e.g., from a DC voltage source, a first switching circuit operable to modulate the DC voltage signal in order to produce a positive pulse width modulated voltage signal for about half the fundamental output period, and a second switching circuit configured to modulate the DC voltage signal for about the other half of the fundamental period. Each switching circuit may also be operable to reverse the polarity of the DC voltage signal so as to reverse the polarity of the pulse width modulated output signal. An output configured between the two switching circuits can be used to provide the output signal to a load.

Another embodiment of the invention provides a system with an input to receive a DC voltage signal, first and second switching circuits electrically coupled to the input, wherein the first switching circuit is operable to produce a positive pulse width modulated output signal as well as operable to reverse the polarity of the DC voltage signal applied to a load during operation. The second switching circuit may be used in a similar fashion so as to reverse polarity at the output and to provide a negative PWM signal at the output.

Other and further advantages and features of the invention will be apparent to those skilled in the art from a consideration of the following description taken in conjunction with the accompanying drawings wherein certain methods and apparatuses for practicing the invention are illustrated. However, it is to be understood that the invention is not limited to the details disclosed but includes all such variations and modifications as fall within the spirit of the invention and the scope of the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a circuit in which a switching circuit modulates an input signal to determine pulse width and spacing of pulses while a second switching circuit controls the polarity of the output signal.

Figure 2 shows the output signal produced by the circuit in Figure 1.

Figure 3 shows the configuration of the circuit in Figure 1 in which the second switching circuit controls the polarity of the output signal while the first switching circuit modulates the input signal to determine pulse width and spacing of pulses.

Figure 4 shows the output signal produced by the circuit in Figure 3.

Figure 5 shows a portion of a pulse width modulation output signal with a superimposed equivalent sine wave that corresponds to the PWM output signal.

Figure 6 shows a conventional bipolar pulse width modulation output signal.

Figure 7 shows a circuit configuration used to produce the output signal shown in Figure 6, wherein a set of switches that operates as a conducting pair and as a non-conducting pair is shown within a dashed border.

Figure 8 shows a configuration of the circuit in Figure 7 wherein the remaining set of switches that operates as a conducting pair and as a non-conducting pair is shown within a dashed border.

Figure 9 shows an embodiment in which a processor provides control signals to an application specific integrated circuit bridge to produce a pulse width modulated output signal that powers a motor.

Figure 10 shows a flow diagram that illustrates the method of operation of producing a pulse width modulated output voltage.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Referring now to Figure 1, an embodiment of the invention can be seen as circuit 100. An inverter circuit is shown having four switches (SW11, SW12, SW21, and SW22). A power supply 102 provides an input voltage to the inverter through an input 107. In addition, an output is established between the switches of the inverters to electrically couple an output signal to the load.

The inverter circuit is preferably an H-bridge inverter circuit comprised of power transistors, such as MOSFET's. Alternatively, other power switching devices could be utilized as well. For example for motor loads of several hundred horsepower, IGBT's may be used or GTO's could be used for motors of several thousand horsepower. The inverter is preferably comprised of two switching circuits. A second switching circuit 204 is comprised of a first switch (SW21) and a second switch (SW22) electrically connected in series. Similarly, a first switching circuit of the inverter circuit is comprised of a first switch (SW11) and a second switch (SW12) electrically connected in series. Preferably, these two switching circuits are connected in parallel. Also, it is preferred that the two switching circuits be electrically coupled in parallel with an input 107 which is shown connected in parallel with the DC voltage source. An output port 108 is preferably established between the two switching circuits 104 and 204. One of the terminals of the input can be grounded so as to establish a reference voltage (Vref) of zero volts. Nevertheless, an offset could also be introduced into the circuit to produce a biased pulse width modulated (PWM) output signal.

Preferably, the input voltage source 102 is a DC voltage source that produces a DC voltage signal for manipulation by the H-bridge inverter circuit. While the phrase DC voltage is used throughout the specification and claims, it should be understood that a pure DC voltage is not required. As those of ordinary skill in the art would understand, practical circuits introduce a ripple into a voltage. So, those voltage signals are intended to be included under the definition of a DC voltage, as well.

The circuit of Figure 1 is utilized to produce the output waveform shown in Figure 2. Often, this waveform is referred to as a partial unipolar pulse width moduated waveform. Figure 2 shows a series of pulses of varying width, but of common voltage magnitude, namely -Vdc. The polarity of the signal in Figure 2, i.e., negative Vdc instead of positive Vdc, is determined by the configuration of the first switching circuit 104. Switch SW12 is shown in a conducting state; thus, it provides a path for a negative DC voltage signal to be applied to the load. The DC voltage signal output across the load will necessarily be -Vdc or zero volts in this configuration. Thus, switches

SW11 and SW12 control the polarity when maintained in opposite conducting and non-conducting states. Thus, in the circuit of Figure 1, the switching circuit 204 actually reverses the voltage of the input voltage +Vdc so that a negative PWM output voltage signal is created, oscillating between –Vdc and 0 volts.

Switching circuit 204 in Figure 1 determines the pulse width and pulse intervals, that is to say, it modulates the input signal to produce the output waveform. Figure 1 shows switches SW21 and SW22 with double headed arrows. This is to indicate that these switches oscillate between conducting and non-conducting states. Preferably, the two switches are not in conducting states simultaneously. Also, it is preferred that when one of these switches is switched from its conducting state to its non-conducting state, that the other switch enter its conducting state from its non-conducting state. Thus, it is preferred to keep these switches in opposite states of conduction when modulating the DC signal.

The width and spacing of the PWM output signal pulses are determined by one of the various PWM schemes. Examples of such schemes are shown, for example, in: "Power Electronics" by Mohan, Undeland, and Robbins, Second Edition, John Wiley and Sons, Inc., 1995, which is hereby incorporated by reference for all that it discloses and for all purposes; "A Centroid-Based PWM Switching Technique for Full-Bridge Inverter Applications" by Ali Yazdian-Varjani et al., in IEEE Transactions on Power Electronics, Vol. 13 No. 1, January 1998, which is hereby incorporated by reference for all that it discloses and for all purposes; "Electrical Machines, Drives, and Power Systems, Fourth Edition," by Theodore Wildi, Prentice Hall, 2000, which is hereby incorporated by reference for all that it discloses and for all purposes. In addition, U.S. Provisional Applications 60/126,770 filed on March 29, 1999, 60/164,083 filed November 5, 1999, 60/163,707 filed November 5, 1999, 60/164,326 filed November 7, 1999 are hereby incorporated by reference in their entirety for all that they disclose and for all purposes. These schemes would be readily understood by one of ordinary skill in the art. Thus, depending on the PWM scheme selected, control signals can be generated and transmitted by a processor to the inverter bridge circuit to control the timing of the operation of the switches. Thus, the opening and closing of switches SW21 and SW22 in Figure 1 produces the pulses and pulse spacing in Figure 2. Namely, switch SW22 is placed in the conducting state and switch SW21 is placed in a non-conducting state when a zero voltage is needed. Alternatively, switch SW22 is placed in a non-conducting state

and switch SW21 is placed in a conducting state when a negative voltage is required to be output.

Figure 3 shows the circuit of Figure 1 configured to produce a positive portion of the unipolar PWM output voltage signal. In Figure 3, switching circuit 204 is placed in the static arrangement where switch SW22 is maintained in a conducting state while switch SW21 is maintained in a non-conducting state. Thus switching circuit 204 is operable to control the polarity of the output signal.

In Figure 3, switching circuit 104 is operable to modulate the input voltage Vdc so as to control the pulse width and pulse spacing of the output voltage pulses. Switches SW11 and SW12 operate in the same fashion as switches SW21 and SW22 operated to produce the negative PWM output waveform. Thus, as can be seen in Figure 4, a positive portion of the unipolar PWM waveform is generated by the circuit shown in Figure 3.

By combining the switch arrangements of Figure 1 and Figure 3, a unipolar pulse width modulated output waveform is generated, as illustrated in Figure 5. Figure 5 also shows a sine wave having a fundamental period (T). This sine wave represents the equivalent sine wave that, in the case of an induction motor load, would cause the induction motor to run at the same speed as that caused by the unipolar pulse width modulated waveform of Figure 5. While the frequency of this equivalent waveform, i.e., the sine wave, is referred to as the fundamental frequency, the frequency of the PWM waveform is referred to as the carrier frequency. Thus, the circuit of Figure 1 is utilized to produce a negative portion of the unipolar pulse width modulated waveform relative to the reference voltage for approximately one half of the fundamental period. Similarly, the circuit of Figure 3 is utilized to produce the positive portion of the unipolar pulse width modulated waveform relative to the reference voltage for approximately the other half of the fundamental period. The switching arrangement can be repreated indefintely for additional periods

Figure 6 illustrates the output voltage produced by conventional systems known as bipolar pulse width modulated voltage signal. As can be seen, the transition of this type of waveform results in a transition of 2Vdc. Thus, as those of ordinary skill in the art would appreciate, the voltage overshoot is twice the magnitute of the transition, namely 4Vdc. In contrast, the unipolar PWM scheme outlined above, would only produce a transition of Vdc and an associated overshoot of 2Vdc across the switch. Thus,

the unipolar scheme is much less damaging to the components of the load, because less voltage is placed across it.

Figures 7 and 8 highlight the association of switches used in the conventional bipolar PWM scheme. As can be seen in Figure 7 and Figure 8, switches SW11 and SW22 operate in unison, while switches SW12 and SW21 also operate in unison. Thus, when SW11 and SW22 are in a conducting state and SW12 and Sw21 are in a non-conducting state, a voltage of +Vdc is applied across the load. Similarly, when SW12 and SW21 are in a conducting state and SW11 and SW22 are in a non-conducting state, as shown in Figure 8, then a voltage of –Vdc is applied across the load. Consequently, in order for a transition of the PWM output signal to occur, all four switches must change state. This creates heat, electrical noise, and shortens the life span of the switches. In contrast, the circuits of Figures 1 and 3 generally only require a transition of two switches in order to cause a transition of the output signal (although 4 additional switch transitions could be required each cycle to account for the two polarity changes each cycle). Thus, the disclosed unipolar PWM switching scheme is accomplished with fewer switch transitions than that required to produce a bipolar pulse width modulated output voltage.

Similarly, in contrast to the unipolar PWM scheme disclosed by Yazdian-Varjani et al., as referenced above, the present unipolar PWM scheme spreads the switching evenly across the four switches of the inverter. In the method of Yazdian-Varjani et al., a single switching circuit was responsible for modulating the DC input signal, while the other switching circuit was solely responsible for controlling the polarity of the output PWM signal. The PWM scheme disclosed herein distributes those responsibilities to both switching circuits. Thus, each switching circuit can be operated to control polarity as well as to modulate the DC voltage signal. Thus, it is advantageous in that it spreads the switching load across all of the switches (SW11, SW12, SW21, and SW22). It also provides symmetry of the two half-bridges. Thus, timing of transistions is simplified because response time of the switches would be similar, as opposed to the system of Yazdian-Varjani et al. in which different switches were proposed for the different half bridges.

The peferred embodiment of the invention has been described with the high side switches (i.e., switches SW11 and SW21 which are electrically coupled to the high side of the power supply) operated so as not to be in a conducting state for a half-cycle of the fundamental output frequency. Rather, as noted in Figure 1 and Figure 3, the

low side switches (SW12 and SW22) are used to control the polarity by remaining on for approximately one half of the fundamental output period. This is yet another advantage over the scheme proposed by Yazdian-Varjani et al. because it typically requires less complicated circuitry to keep the low side switches in a conducting state as compared to the high side switches. For example, a lower cost "boot strap supply" can be used for the high side FET gate drivers in this preferred embodiment. Nevertheless, it should be understood that one might choose to reverse the conduction states of switches SW11 and SW12 in Figure 1 and SW21 and SW22 in Figure 3. Thus, such an alternative embodiment would also be covered by this invention.

Figure 9 shows an embodiment in which the inverter bridge circuit is configured as part of an application specific integrated circuit, as would be understood by a person of ordinary skill in the art. The ASIC may either house just the power transistors, or it may be configured with a microprocessor so as to allow the control signals for the switches to be routed directly to the power transistors without any external wiring. In Figure 9, a microprocessor is shown separate from the ASIC. Similarly, the ASIC could also include a power supply or power conversion circuit to produce the DC waveform utilized in creating a pulse width modulated output.

Figure 10 illustrates a method 1000 for implementing an embodiment of the invention. As shown in Figure 10, a DC voltage signal is provided 1004. One may utilize a two switch network as a first switching circuit 1008 and utilize a two switch network as a second switching circuit 1012. The switching circuits are preferably electrically coupled in parallel with the DC voltage signal 1016. Also, an output is configured between the first and second switching circuits 1020. The first switching circuit is utilized to modulate the DC voltage signal so as to produce a positive PWM output signal for about one half of the fundamental output period 1024. In additon, the first switching circuit is utilized to reverse the polarity of the DC signal applied to the output so as to revese the polarity of the PWM output signal 1028. Similarly, the second switching circuit is utilized to switch the DC voltage signal so as to produce a negative PWM output signal for the other half of the fundamental output period 1032. Also, the second switching circuit is utilized to reverse the polarity of the DC signal applied to the output so as to reverse the polarity of the PWM output signal 1036. The load is powered with the generated output signal 1040.

In addition to embodiments where the invention is accomplished by hardware, it is also noted that these embodiments can be accomplished through the use of

an article of manufacture comprised of a computer usable medium having a computer readable program code embodied therein, which causes the enablement of the functions disclosed in this description. For example, this might be accomplished through the use of hardware description language (HDL), register transfer language (RTL), VERILOG, VHDL or similar programming tools, as one of ordinary skill in the art would understand. It is therefore envisioned that the functions accomplished by the present invention as described above could be represented in a core which could be utilized in programming code and transformed to hardware as part of the production of integrated circuits. Therefore, it is desired that the embodiments expressed above also be considered protected by this patent in their program code means as well.

It is also noted that many of the structures and acts recited herein can be recited as means for performing a function or steps for performing a function, respectively. Therefore, it should be understood that such language is entitled to cover all such structures or acts disclosed within this specification and their equivalents, including the matter incorporated by reference.

It is thought that the apparatuses and methods of the embodiments of the present invention and many of its attendant advantages will be understood from the foregoing description. It will be apparent that various changes may be made in the form, construction and arrangement of the parts thereof without departing from the spirit and scope of the invention or sacrificing all of its material advantages, the form hereinbefore described being merely a preferred or exemplary embodiment thereof.

WHAT IS CLAIMED IS:

1. A method comprising:

providing a DC voltage signal;

utilizing a first switching circuit (104) to switch said DC voltage signal so as to produce relative to a reference voltage a positive pulse width modulated voltage signal for about one half of a fundamental output period;

utilizing a second switching circuit (204) to switch said DC voltage signal so as to produce relative to said reference voltage a negative pulse width modulated voltage signal for about one half of said fundamental output period.

2. The method as described in claim 1 and further comprising:

reversing the polarity of said DC voltage signal after switching said DC voltage signal for about one half of said fundamental output period.

3. The method as described in claim 2 and further comprising utilizing said first switching circuit (104) to reverse the polarity of said DC voltage signal.

4. The method as described in claim 2 and further comprising utilizing said second switching circuit (204) to reverse the polarity of said DC voltage signal.

5. The method as described in claim 1 and further comprising:

utilizing a two switch network (SW11, SW12) as said first switching circuit;

electrically coupling said two switch network in parallel with said DC voltage signal;

utilizing a two switch network (SW21, SW22) as said second switching circuit;

electrically coupling said two switch network of said second switching circuit in parallel with said DC voltage signal;

configuring an output (108) between said two switch network of said first switching circuit and said two switch network of said second switching circuit.

6. An apparatus comprising:

an input (108) to receive a DC voltage signal;

a first switching circuit (104) configured to modulate said DC voltage signal so as to produce relative to a reference voltage a positive pulse width modulated voltage signal for about one half of a fundamental output period;

a second switching circuit (204) configured to modulate said DC voltage signal so as to produce relative to said reference signal a negative pulse width modulated voltage signal for about one half of said fundamental output period.

7. The apparatus as described in claim 6 and further comprising a circuit operable to reverse the polarity of said DC voltage signal.

8. The apparatus as described in claim 7 wherein said first switching circuit (104) is operable to reverse the polarity of said DC voltage signal.

9. The apparatus as described in claim 7 wherein said second switching circuit (204) is operable to reverse the polarity of said DC voltage signal.

10. The apparatus as described in claim 6 wherein said first switching circuit comprises a two switch network in parallel with said DC voltage signal and wherein said second switching circuit comprises a two switch network in parallel with said DC voltage signal; and further comprising an output (108) electrically coupled between said two switch network of said first switching circuit and said two switch network of said second switching circuit.

11. An apparatus for providing a pulse width modulated voltage signal, said apparatus comprising:

an input (107) to receive a DC voltage signal;

a first switching circuit (104) electrically coupled to said input so as to be electrically coupled to said DC voltage signal during operation;

a second switching circuit (204) electrically coupled to said input so as to be electrically coupled to said DC voltage signal during operation;

wherein said first switching circuit (104) is operable to produce a positive pulse width modulated output signal relative to a reference voltage; and

wherein said first switching circuit (104) is operable to reverse the polarity of said DC voltage signal applied to a load during operation.

12. The apparatus as described in claim 11 wherein said second switching circuit (204) is operable to produce a negative pulse width modulated output signal relative to said reference voltage.

13. The apparatus as described in claim 12 wherein said second switching circuit (204) is operable to reverse the polarity of said DC voltage signal.

14. The apparatus as described in claim 11 wherein said first switching circuit comprises a first switch and a second switch , said first switch and second switch operable

to reverse said polarity of said DC voltage signal when said first switch is placed in a conducting state and said second switch is placed in a non-conducting state.

15. The apparatus as described in claim 11 wherein said input is electrically coupled in parallel with said first switching circuit and said second switching circuit.

16. A method of providing a pulse width modulated output voltage signal, said method comprising:

providing a DC voltage signal;

providing a first switching circuit (104) electrically coupled to said DC voltage signal;

providing a second switching circuit (204) electrically coupled to said DC voltage signal;

operating said first switching circuit (104) to produce a positive pulse width modulated output signal relative to a reference voltage;

operating said first switching circuit to reverse the polarity of said positive pulse width modulated output signal once during a fundamental output period.

17. The method as described in claim 16 and further comprising:

operating said second switching circuit to produce a negative pulse width modulated output signal relative to said reference voltage.

18. The method as described in claim 17 and further comprising:

operating said second switching circuit (204) to reverse the polarity of said output signal.

19. The method as described in claim 16 wherein said first switching circuit (104) comprises a first switch and a second switch, said method further comprising:

reversing the polarity of said positive pulse width modulated output signal by maintaining said first switch in a non-conducting state while maintaining said second switch in a conducting state.

20. The method as described in claim 16 and further comprising:

electrically coupling said DC voltage signal in parallel with said first switching circuit; and

electrically coupling said DC voltage signal in parallel with said second switching circuit.

21. An apparatus to generate a pulse width modulated voltage signal, said apparatus comprising:

a DC voltage source (102);

a first switching circuit (104) comprising a first switch and a second switch configured in a series circuit, said first switching circuit electrically coupled in parallel with said DC voltage source;

a second switching circuit (204) comprising a third switch and a fourth switch configured in a series circuit, said second switching circuit electrically coupled in parallel with said DC voltage source;

an output (108) comprising a first electrical junction coupling said first switch with said second switch and a second electrical junction coupling said third switch with said fourth switch;

said second switching circuit (204) operable to maintain said third switch in a conducting state while said fourth switch is maintained in a non-conducting state so as to establish a first polarity of an output signal;

said first switching circuit operable to switch said first switch and said second switch at a modulation frequency;

said first switching circuit operable to maintain said second switch in a conducting state while maintaining said first switch in a non-conducting state so as to establish a second polarity of said output signal, said second polarity being the reverse polarity of said first polarity; and

said second switching circuit operable to switch said third switch and said fourth switch at said modulation frequency.

22. The apparatus as described in claim 21 wherein said first switching circuit and said second switching circuit are configured as part of an application specific integrated circuit.

23. The apparatus as described in claim 21 wherein said first switching circuit (104) is operable to produce a positive pulse width modulated output signal during about one half cycle of a fundamental output period; and

wherein said second switching circuit (204) is operable to produce a negative pulse width modulated output signal during the other half cycle of said fundamental output period.

24. The apparatus as described in claim 21 and further comprising a motor electrically coupled to said output.

25. The apparatus as described in claim 21 and further comprising a microprocessor electrically coupled to said first switching circuit and to said second switching circuit, said microprocessor operable to control said first switching circuit and said second switching circuit.

26. A method of generating a pulse width modulated voltage signal, said method comprising:

providing a DC voltage source (102);

electrically coupling said DC voltage source in parallel with a first switching circuit (104) comprising a first switch and a second switch configured in a series circuit;

electrically coupling said DC voltage source in parallel with a second switching circuit (204) comprising a third switch and a fourth switch configured in a series circuit;

establishing an output (108) comprising a first electrical junction coupling said first switch and said second switch and a second electrical junction coupling said third switch and said fourth switch;

maintaining said third switch in a conducting state while maintaining said fourth switch in a non-conducting state so as to establish a first polarity of an output signal;

switching said first switch and said second switch at a modulation frequency; then

maintaining said second switch in a conducting state while maintaining said first switch in a non-conducting state so as to establish a second polarity of said output signal, said second polarity being the reverse polarity of said first polarity;

switching said third switch and said fourth switch at said modulation frequency.

27. The method as described in claim 26 and further comprising:

configuring said first switching circuit and said second switching circuit as part of an application specific integrated circuit.

28. The method as described in claim 26 and further comprising:

utilizing said first switching circuit to produce a positive pulse width modulated output signal during about one half cycle of a fundamental output period; and

utilizing said second switching circuit to produce a negative pulse width modulated output signal during the other half cycle of said fundamental output period.

29. The method as described in claim 26 and further comprising powering a motor with said output signal.

30. The method as described in claim 26 and further comprising controlling said first switching circuit and said second switching circuit with a processor.

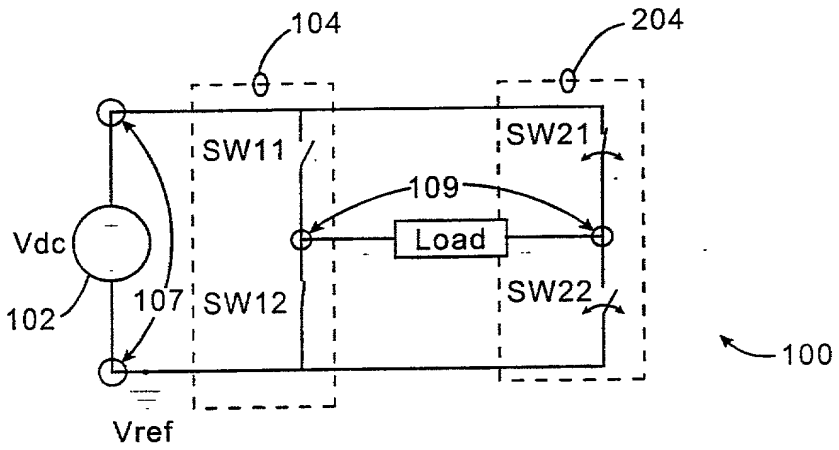
104
204
SW11
SW21
109
Load
Vdc
102
107
SW12
SW22
100
Vref

FIG. 1

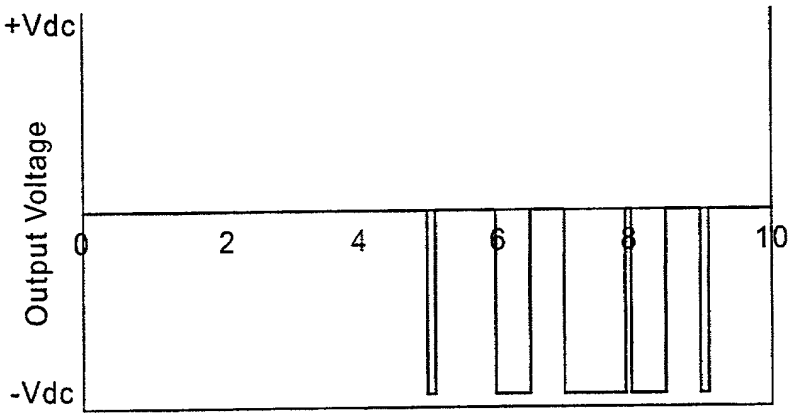
+Vdc
Output Voltage
0
2
4
6
8
10
-Vdc

FIG. 2

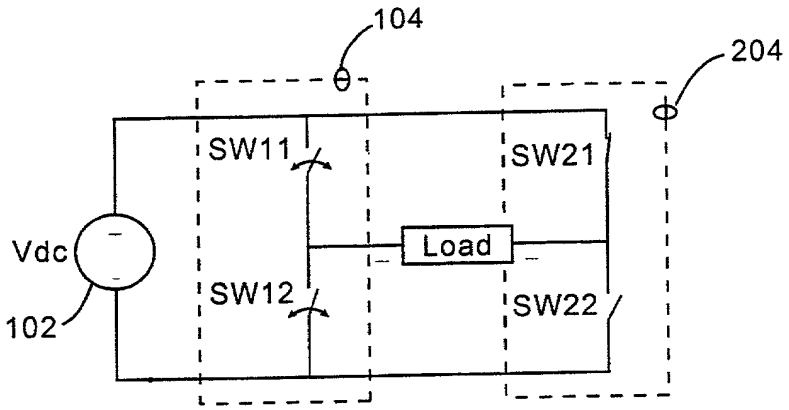
104
204
SW11
SW21
Vdc
Load
SW12
SW22
102

FIG. 3

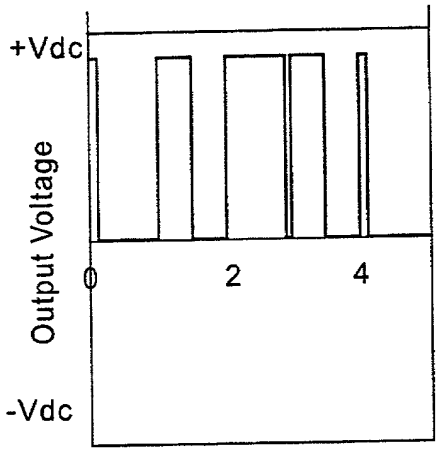
+Vdc
Output Voltage
0
2
4
-Vdc

FIG. 4

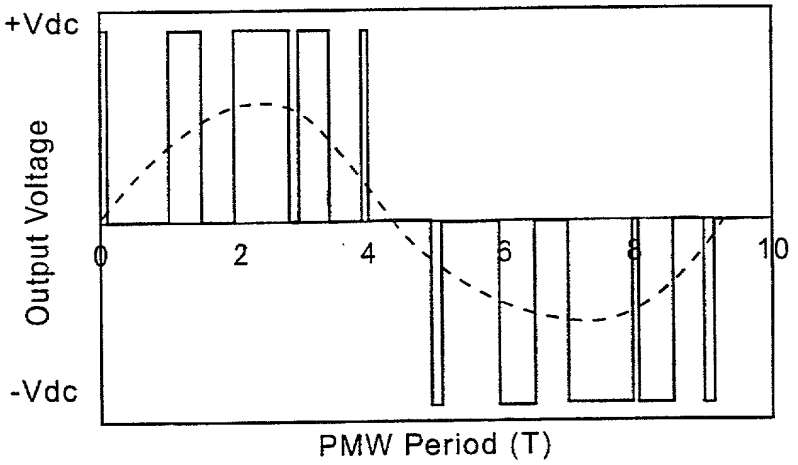
+Vdc
Output Voltage
-Vdc
0
2
4
6
8
10
PMW Period (T)

FIG. 5

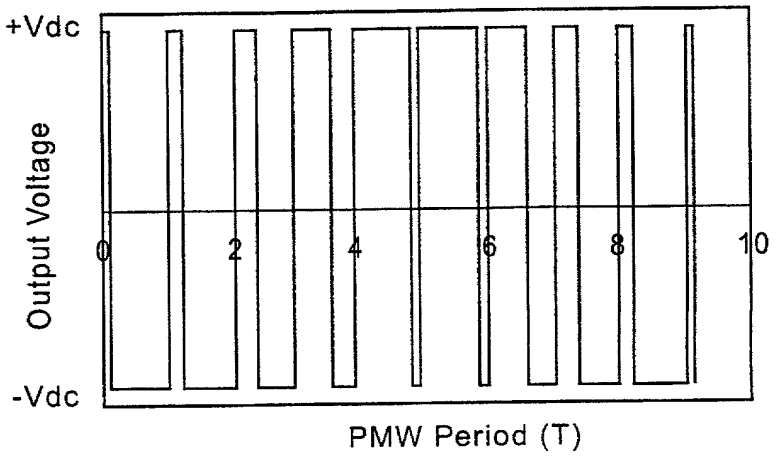
+Vdc
Output Voltage
-Vdc
0
2
4
6
8
10
PMW Period (T)

FIG. 6

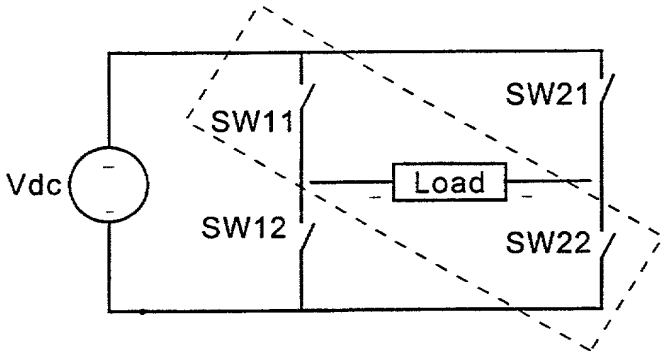

FIG. 7

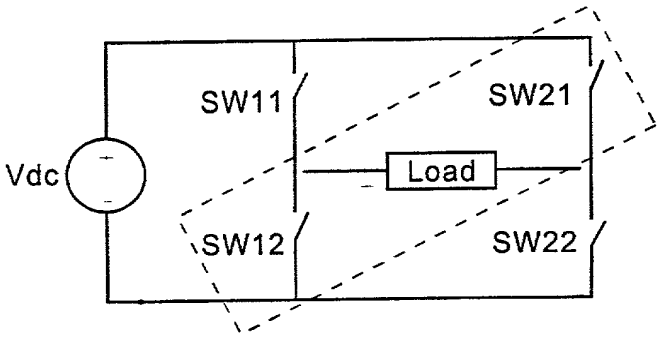

FIG. 8

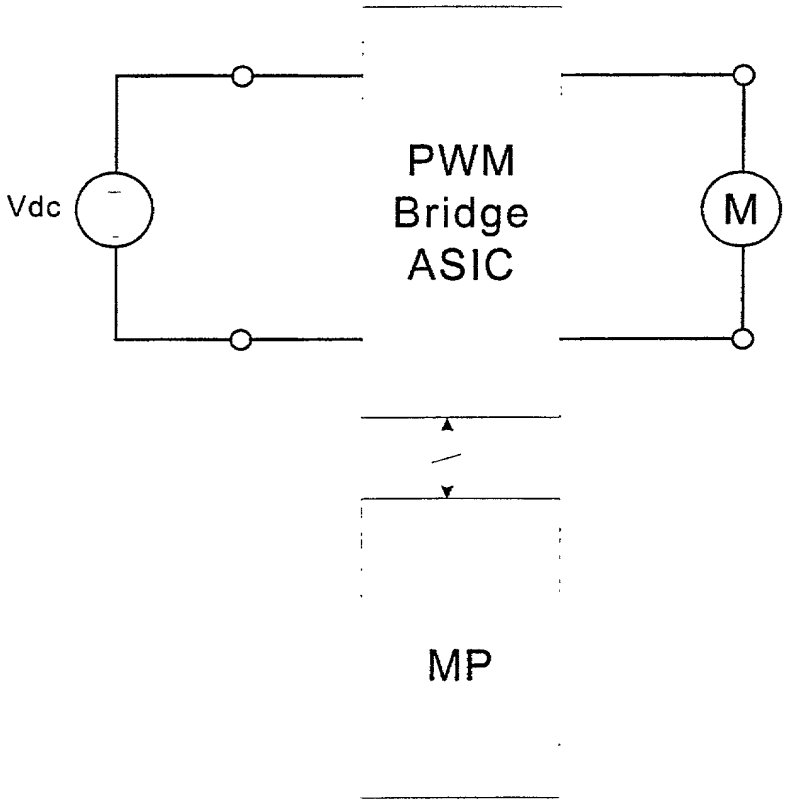

FIG. 9

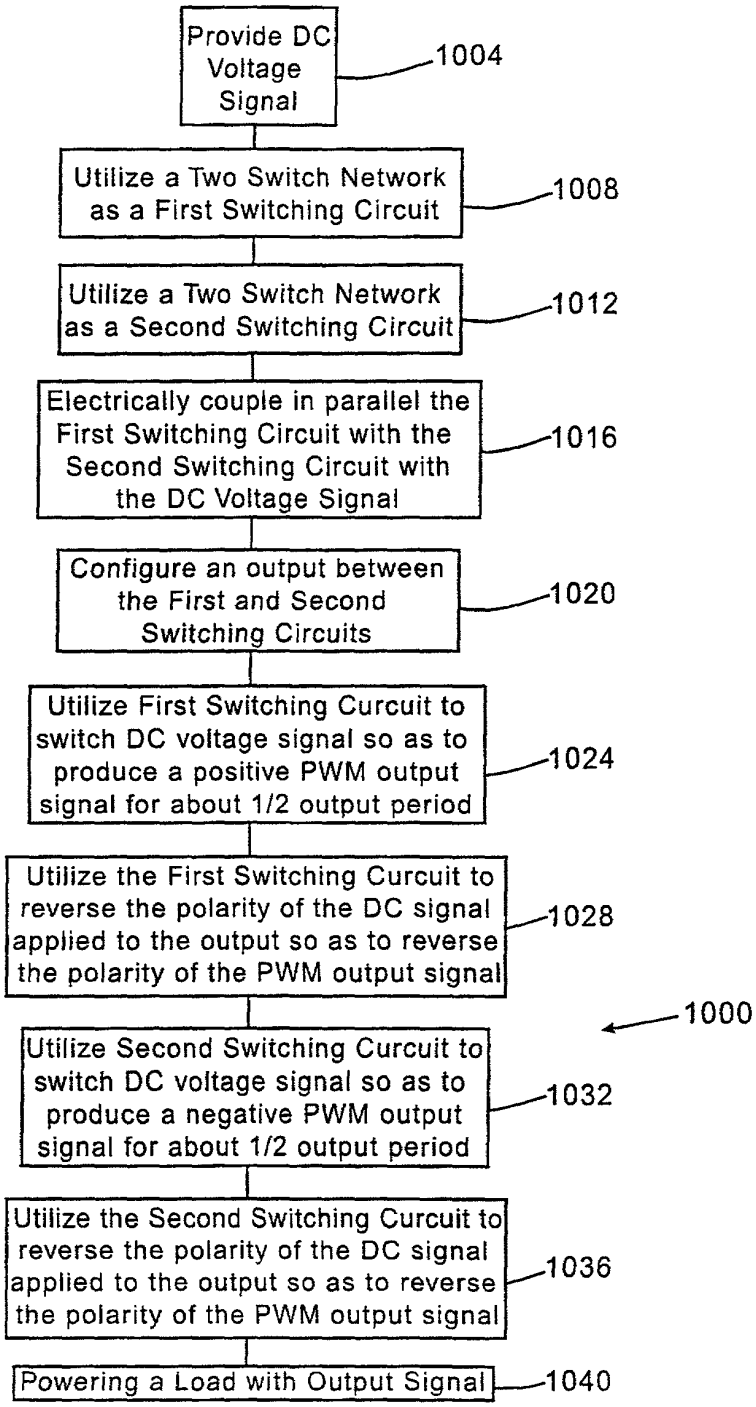
Provide DC Voltage Signal
1004
Utilize a Two Switch Network as a First Switching Circuit
1008
Utilize a Two Switch Network as a Second Switching Circuit
1012
Electrically couple in parallel the First Switching Circuit with the Second Switching Circuit with the DC Voltage Signal
1016
Configure an output between the First and Second Switching Circuits
1020
Utilize First Switching Curcuit to switch DC voltage signal so as to produce a positive PWM output signal for about 1/2 output period
1024
Utilize the First Switching Curcuit to reverse the polarity of the DC signal applied to the output so as to reverse the polarity of the PWM output signal
1028
1000
Utilize Second Switching Curcuit to switch DC voltage signal so as to produce a negative PWM output signal for about 1/2 output period
1032
Utilize the Second Switching Curcuit to reverse the polarity of the DC signal applied to the output so as to reverse the polarity of the PWM output signal
1036
Powering a Load with Output Signal
1040

FIG. 10

Please type a plus sign (+) inside this box → [+] →

PTO/SB/01 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted With Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)

Attorney Docket Number	19730-000110US
First Named Inventor	ANSARI, Zahid
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ANSARI, Zahid
PRICKETT, Bruce L.
GUY, Jonathan Andrew

METHOD AND APPARATUS FOR PROVIDING PULSE WIDTH MODULATION *(Title of the Invention)*
the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 28/03/2000 as United States Application Number or PCT International

Application Number ____ and was amended on (MM/DD/YYYY) ____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

Please type a plus sign (+) inside this box → +

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this unsigned inventor

1-00

Zarlé | ANSARI
Given Name (first and middle [if any]) | Family Name or Surname

Inventor's Signature [signature] | 8 OCT 2001 Date

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Mailing Address

Menlo Park City | CA State | 94025 ZIP | US COUNTRY

NAME OF SECOND INVENTOR: ☐ A petition has been filed for this unsigned inventor

2-00

Bruce L. | PRICKETT
Given Name (first and middle [if any]) | Family Name or Surname

Inventor's Signature [signature] | 9 Oct 2001 Date

Fremont Residence: City | CA State CA. | US Country | US Citizenship

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Fremont City | CA State | 94539 ZIP | US COUNTRY

☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

PTO/SB/02A (10-00)

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 1 of 1

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Jonathan Andrew	GUY		
Inventor's Signature			Date 9-28-01
Residence: City Austin	State TX	Country US	Citizenship NZ
Mailing Address 4444 Bremner Drive			
City Austin	State TX	ZIP 78749	Country US
Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
Mailing Address			
City	State	ZIP	Country
Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])	Family Name or Surname		
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
Mailing Address			
City	State	ZIP	Country

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DE 7051369 v1

Atty. Docket No. 019730-000110US

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(b)) - NON-INVENTOR

Applicant or Patentee: ANSARI, et al./Anacon Systems, Inc.
Application or Patent No.:
Filed or Issued:
Title: METHOD AND APPRATUS FOR PROVIDING PULSE WIDTH MODULATION

I hereby declare that I am making this verified statement to support a claim by Anacon Systems, Inc. for small entity status for purposes of paying reduced fees to the United States Patent and Trademark Office, regarding the invention described in:

- ☒ the specification filed herewith with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

I hereby declare that I would qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying fees to the United States Patent and Trademark Office, if I had made the above-identified invention.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey or license any rights in the invention is listed below:*

- ☐ No such person, concern, or organization
- ☐ Persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name
Address

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Name
Address

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Name
Address

☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Person Signing: Bala Padmakumar
Title of Person if Other than Owner: President
Address of Person Signing: 1043 Shoreline Boulevard, Suite 202, Mountain View, CA 94303

SIGNATURE _____ DATE 9/27/01